New Strategies and Concepts in Automotive Embedded System Development

PART II

Ateliers Electroniques Automobile 2005

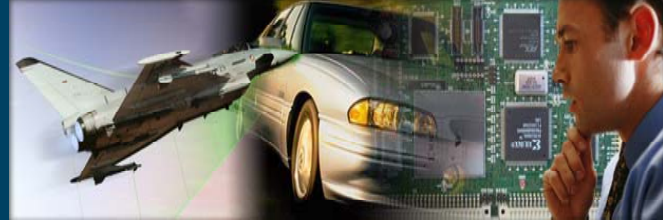
Jouy-en-Josas, Le 17 novembre 2005 au Domaine du Montcel

Dr. Karlheinz E. Weiss

X2E GmbH

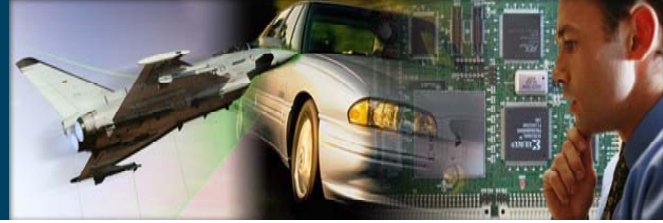
embedded system design

Overview



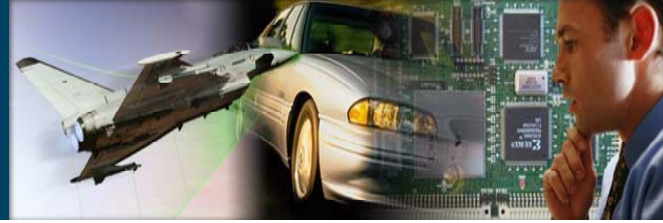
- Introduction
  - Future requirements in automotive embedded system design
  - Basics of Field Programmble Gate Arrays (FPGA)
  - Development tool flow for System on a Chip (SoC)-FPGA
- FPGA contra ASIC development
- Application Example: Complex Gateway
  - FPGA based Standard Core
  - Low cost FPGAs based on soft processors
- Conclusion
- Outlook

Introduction
Future Requirements

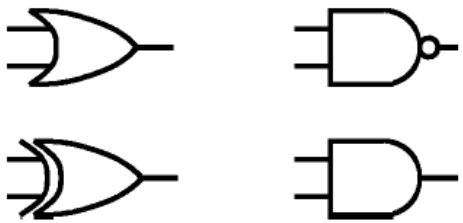


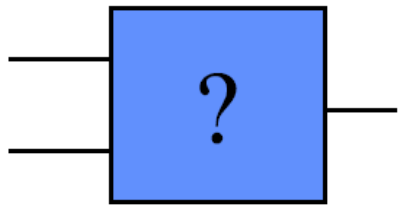
- Electronic devices dramatically increases the „added value“ of the car
- Developing cycles will be shorten in the future
- System integration will become the main challenge for the OEM
  - Requires more time and effort before start of production
- Costs must be reduced
- Development risks and time must be reduced
- What ist required in the future? New Strategies and Concepts, based on
  - New technologies: Programmable Logic (e.g.: SoC FPGAs)
  - High level design re-use
  - Rapid prototyping methods
  - Powerfull tool support

Introduction
Basics of FGPA



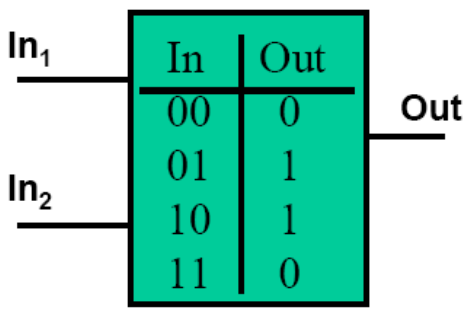
Amount of programmable logic gates, integrated into a flexible connection network is called: „user programmable“ alternative to a dedicated integrated circuit



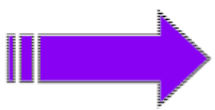


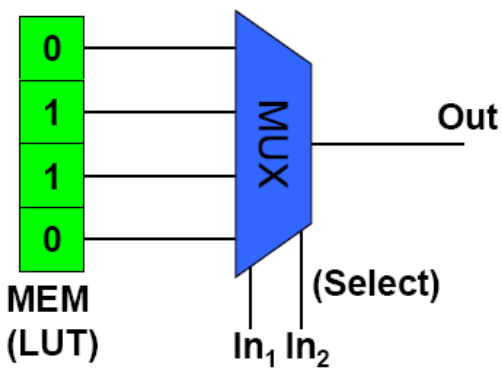
Programmable Gate: How does it work?

Lösung:

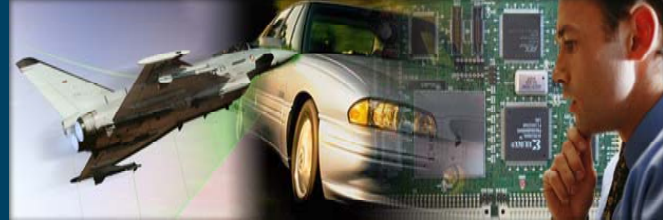


Look-up-Table (LUT) mit 2 Eingängen



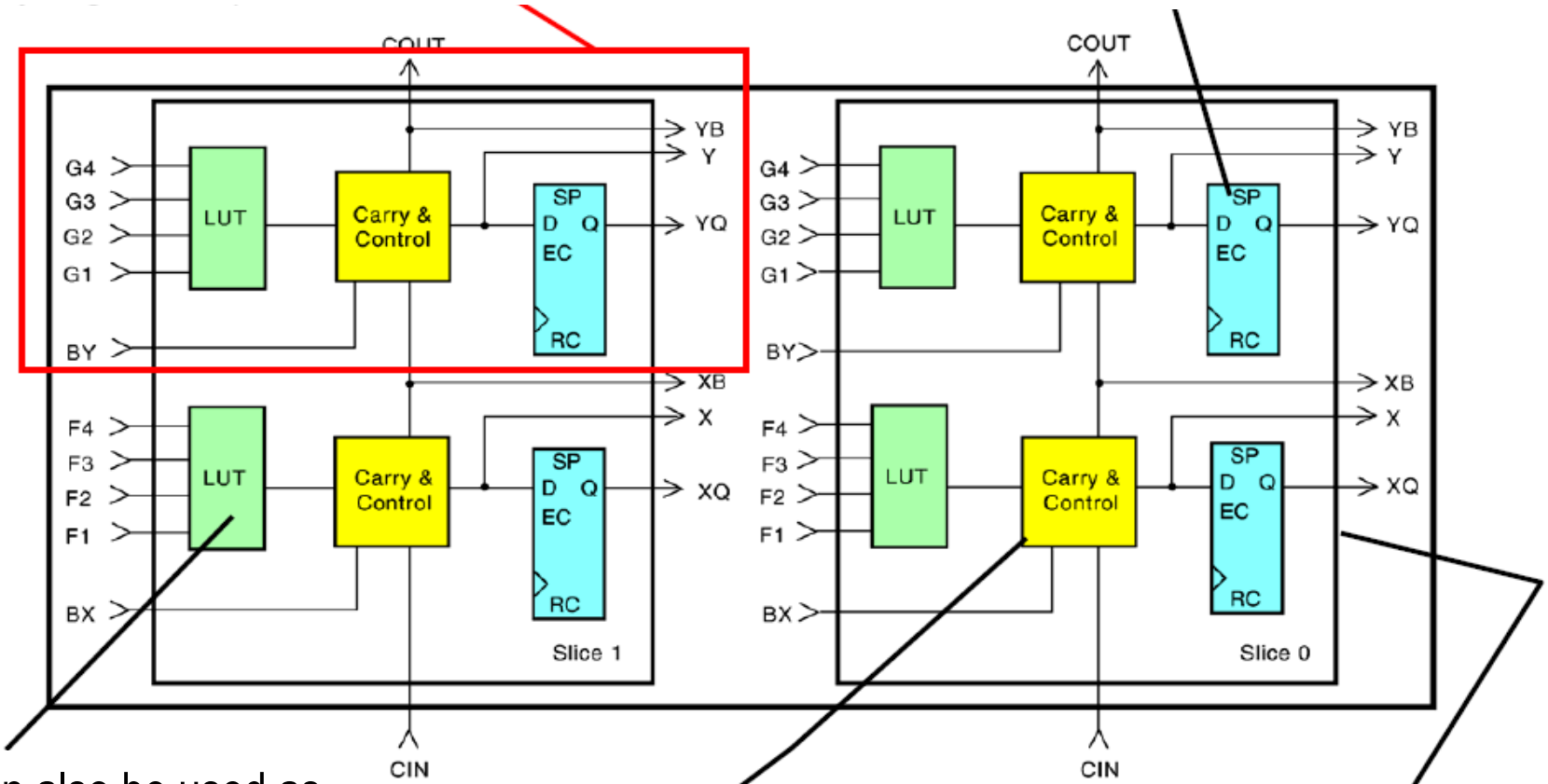


Introduction
Basics of FGPA



Logic Cell, based on one LUT with 4 inputs,
One fast carry logic and one FF

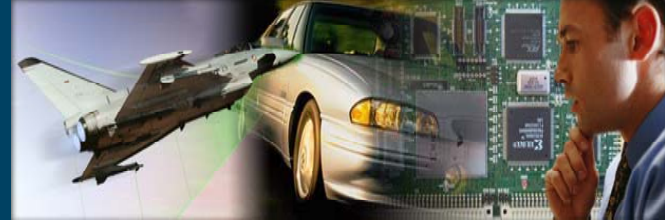
FF can be used as a D-FF
or a level triggert Latch

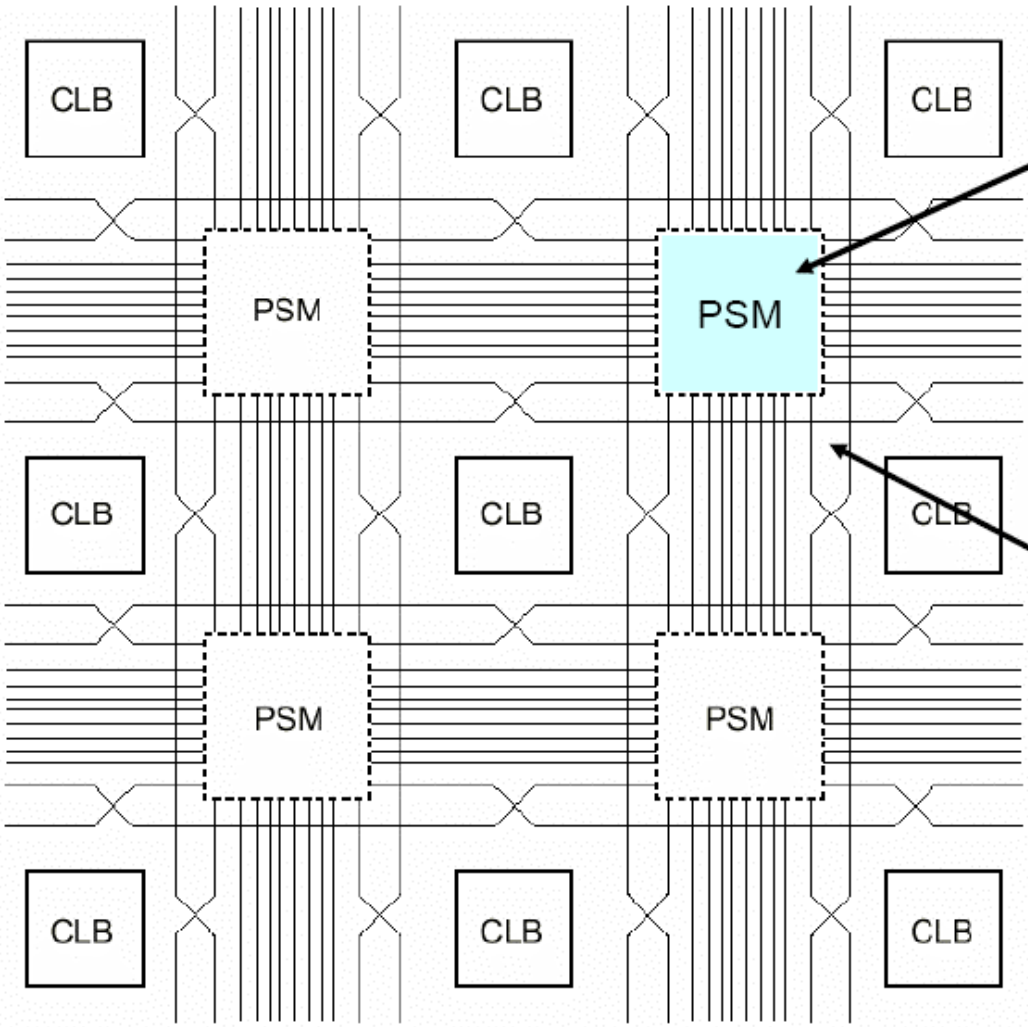


LUT can also be used as
16 Bit SRAM memory

One entire Complex Logic Block (CLB) is
based on 4 Logic Cells: Called 2 Slices

Introduction
Basics of FGPA

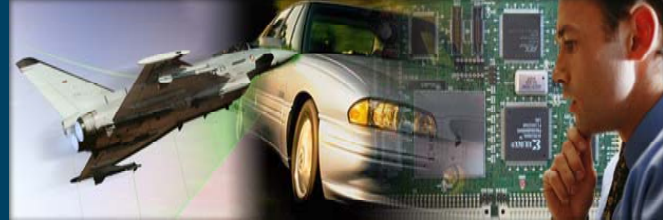




- FPGA Chip Architecture
- PSM = Programmable Switch Matrix
- CLB = Complex Logic Block
- LUT = Look Up Tables, main parts inside the CLB
- Horizontal and vertical metal lines, connected trough pass transistors inside the PSM,
- Connection and logic information stored into SRAM cells: called FPGA configuration,
- FPGA boot up after power on (e.g. from Flash, 10ms, about 500kB)

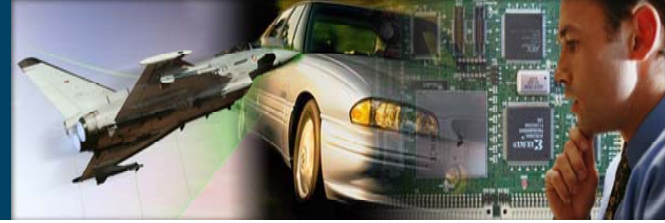
embedded system design

Introduction
Basic Terms

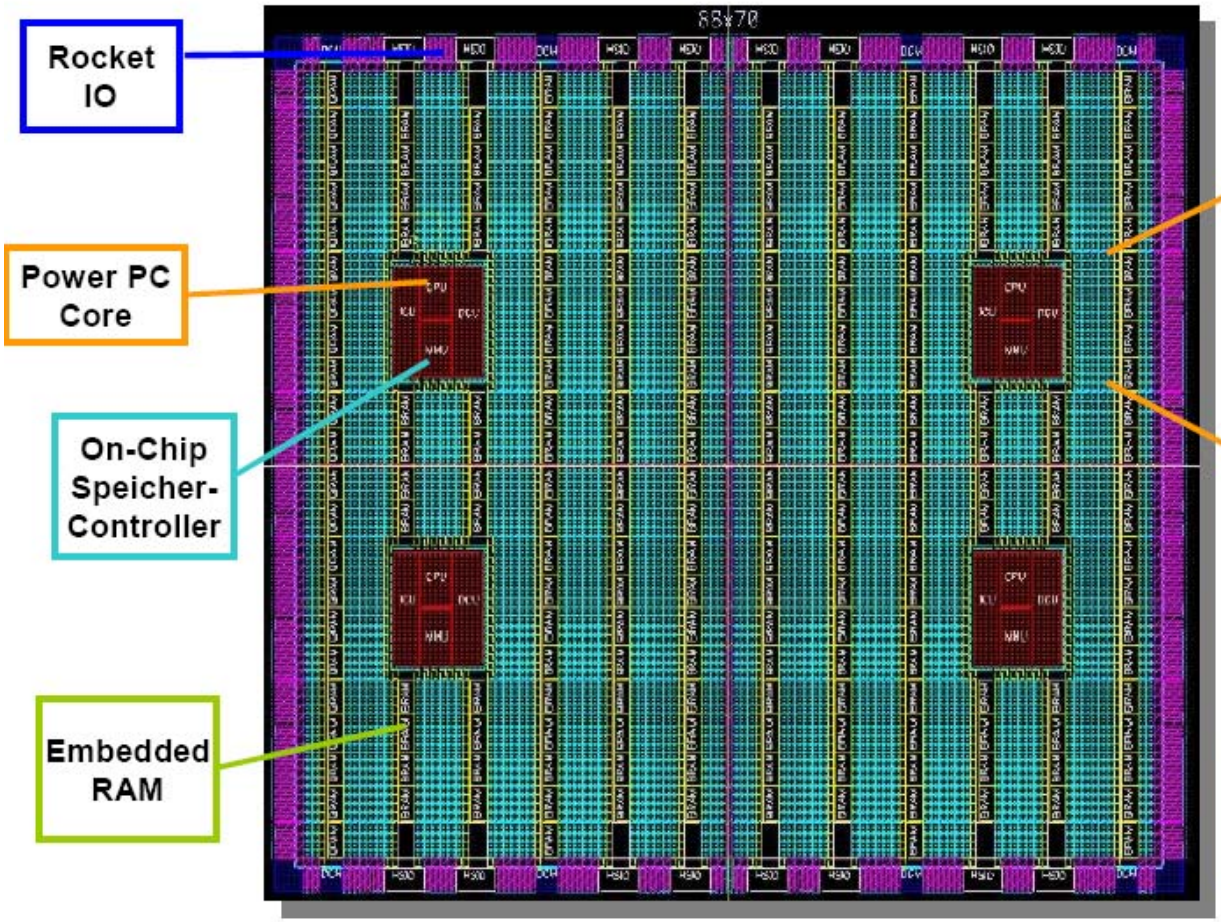


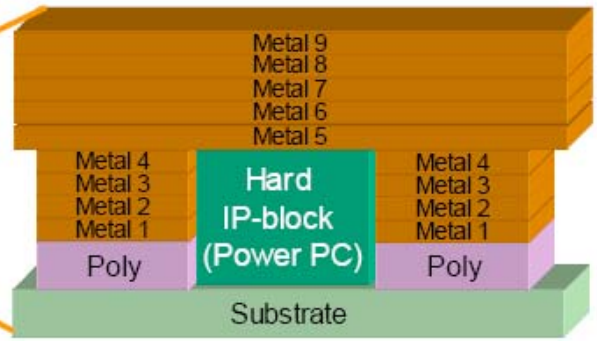
- VHDL: **V**ery high speed integrated circuits **H**ardware **D**escription **L**anguage
  - Used to describe the behaviour of a complex functionality intended for the implementation in a “piece of hardware onto a chip (e.g. FPGA, ASIC)
- IP-core: **I**ntellectual **P**roperty
  - Digital Hardware function block (e.g. CAN, MOST, FlexRay, Ethernet, Processor etc.) described in VHDL, typically available in a appropriate design library
  - Hard-IP: Hardware function block, fixed implemented and wired at a chip – hard-IP needs no programmable resources (e.g. PPC405 core inside the Virtex SoC FPGAs
  - Soft-IP: Hardware function block, described in VHDL, can be synthesized towards a dedicated target technology (e.g. FPGA, soft-IP needs programmable resources)

Introduction
SoC FPGA and Tools



Virtex-II FPGA: integrierte PowerPC ® 405 RISC CPUs (PPC405)





	Fastest DSP	Virtex-II
8x8 MAC	4.8 Billion MAC/s	0.5 Tera MAC/s
256-FIR	9.3 MSPS	180 MSPS
1024-FFT	10 µs	1 µs

embedded system design

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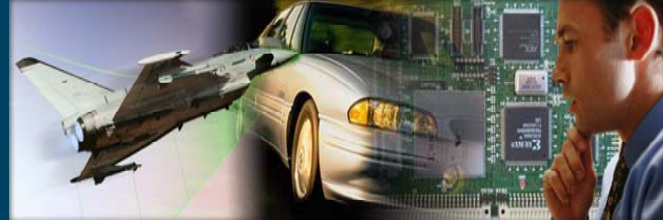
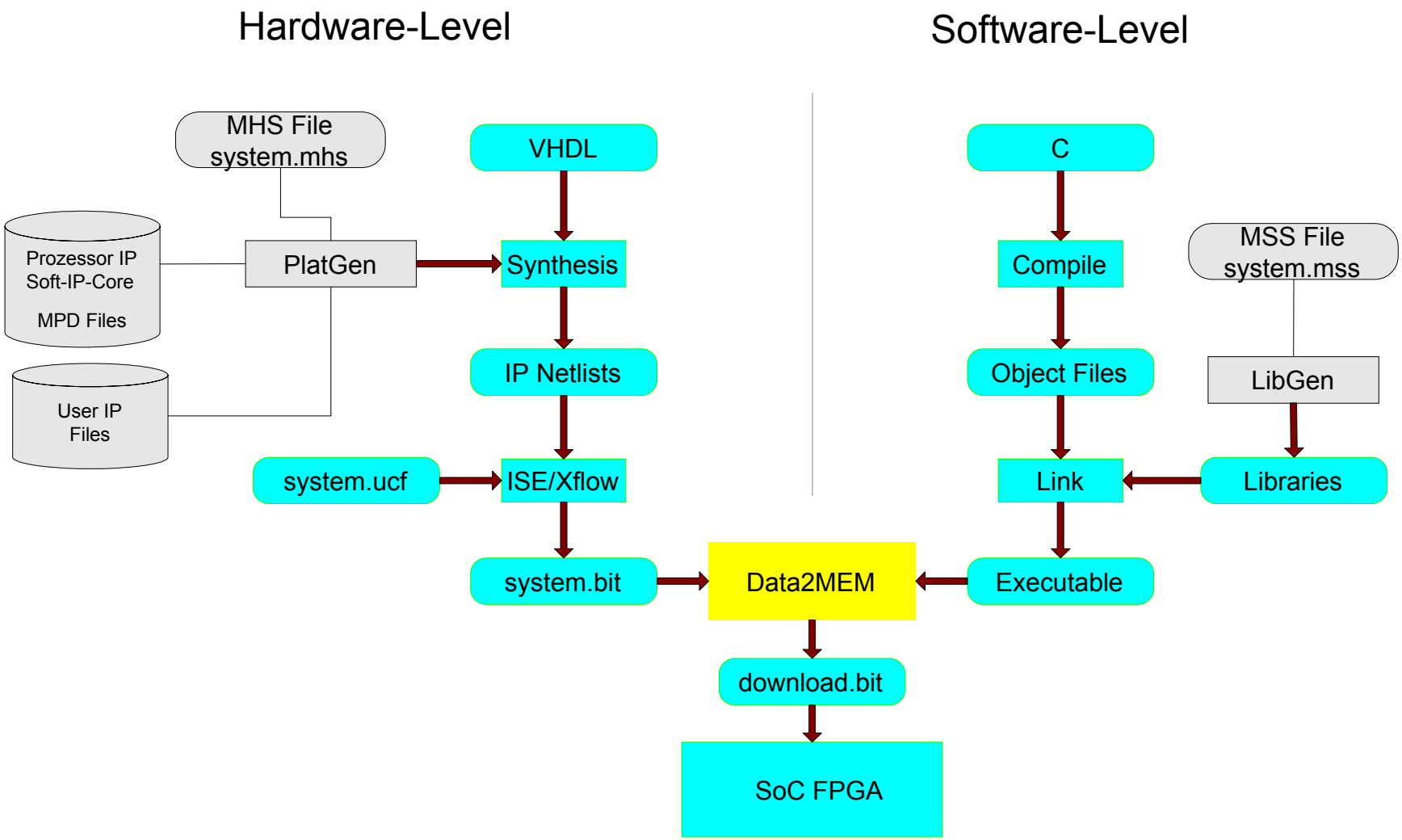
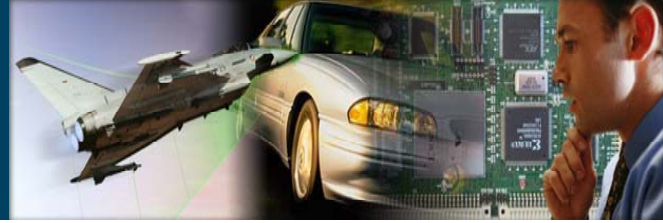
SoC FPGA and Tools





FPGA contra ASIC development



- System on Chip Field Programmable Gate Arrays (SoC-FPGA)
- Advantages
  - Fast time to Market
  - Shorter Design Cycles
  - Hardware Updates
  - Less design risks
  - Long term availability
  - Easier IP re-use
  - „Early hardware availability“
- Disadvantages
  - Additional effort and time for configuration
  - Higher cost per gate

- Application Specific Integrated Circuits (ASIC)
- Advantages
  - Highest possible integration level
  - Lower cost per gate
  - No configuration necessary
- Disadvantages
  - Potential design risk
  - Higher initial develpment cost
  - Longer time to market
  - „Late hardware availability“

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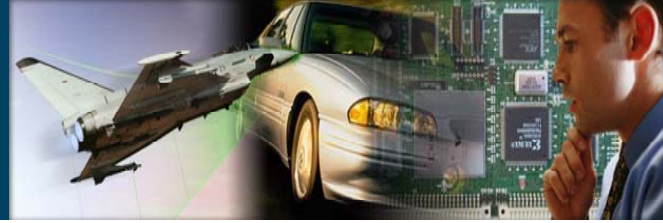
Application Example
Low Cost Gateway



Embedded Bios & RTC

RTA-OSEK

Control HMI Left

Control HMI Right

simple test and routing layer

TCP/IP

Netzwerkmanagement

NetServices V2.x

FlexRayDriver

Ethernet Driver

CAN Driver

MOST Low Level Driver

OSEK Board Support Package

SoC FPGA SPARTAN III E (32 Bit MicroBlaze Soft-Processor)

Page Mode Flash/SRAM EMC
Terminal UART & JTAG/BDM
Interrupt-Controller

Full Ethernet IP Core

6 x CAN IP Core

MediaLB IP Core

FlexRay Internal IP-Core

2 x LIN IP-Core

4MB Flash with Fast Page Mode

1MB asyn. SRAM

Phy & RJ45 Header

5 x high speed, 1 x low speed transceivers

OS81050 INIC

MicroPigtal 2-0 FOT

10MBit transceiver

2 x transceiver

BMW & BMW CarIT

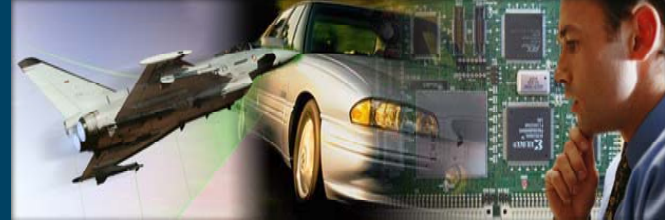
Life Devices (ETAS)

X2E

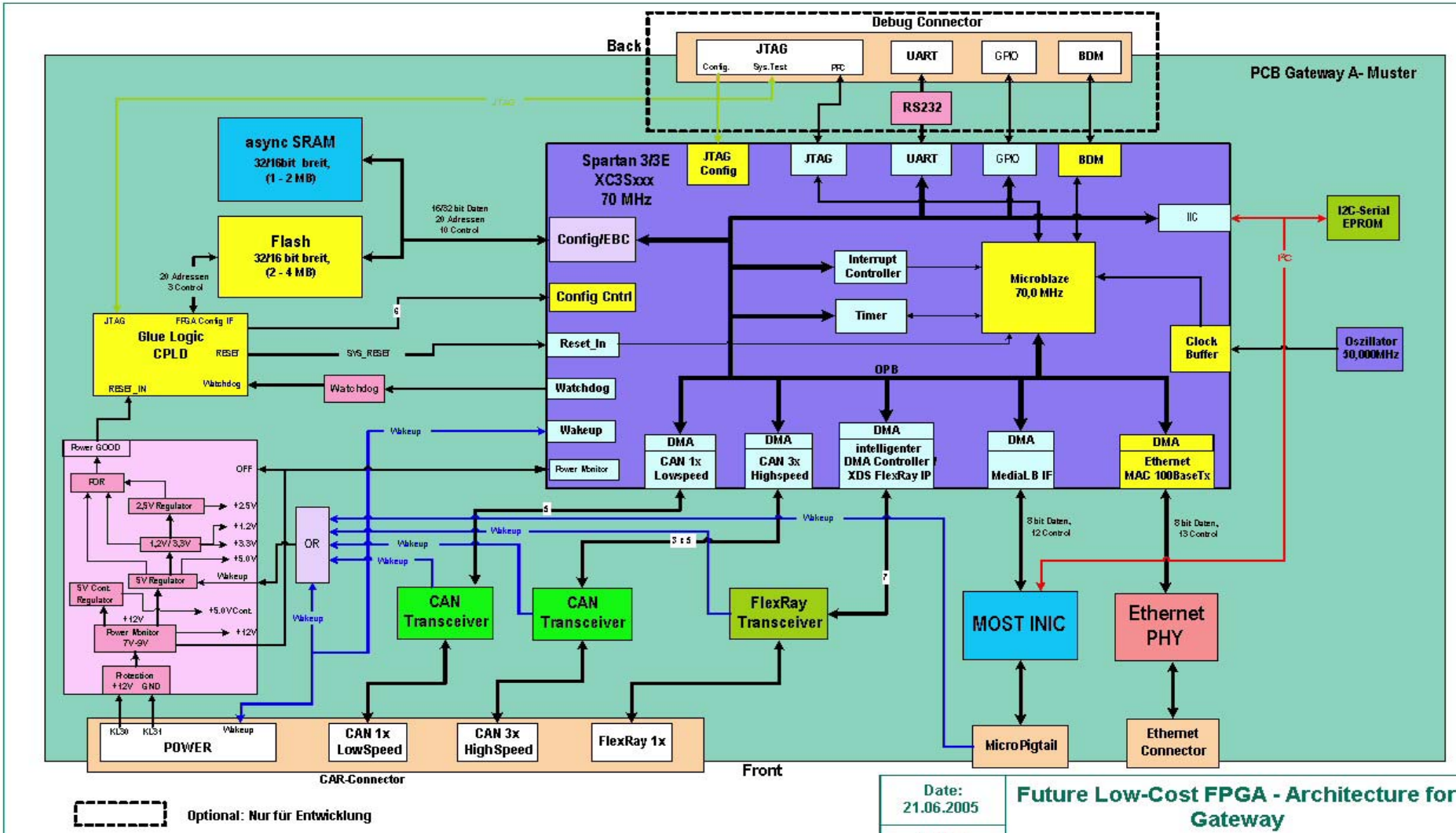
OASIS Silicon Systems

XILINX

Application Example
Low Cost Gateway



embedded system design



Date: 21.06.2005	Future Low-Cost FPGA - Architecture for Gateway
Author: Carsten Oetker	
Version: 1.0	Department X2E GmbH

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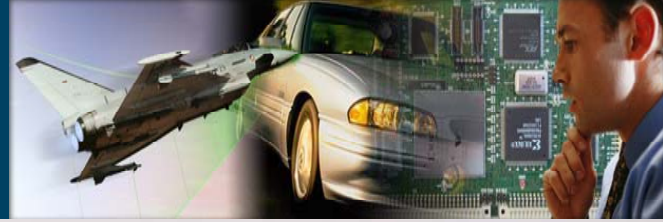
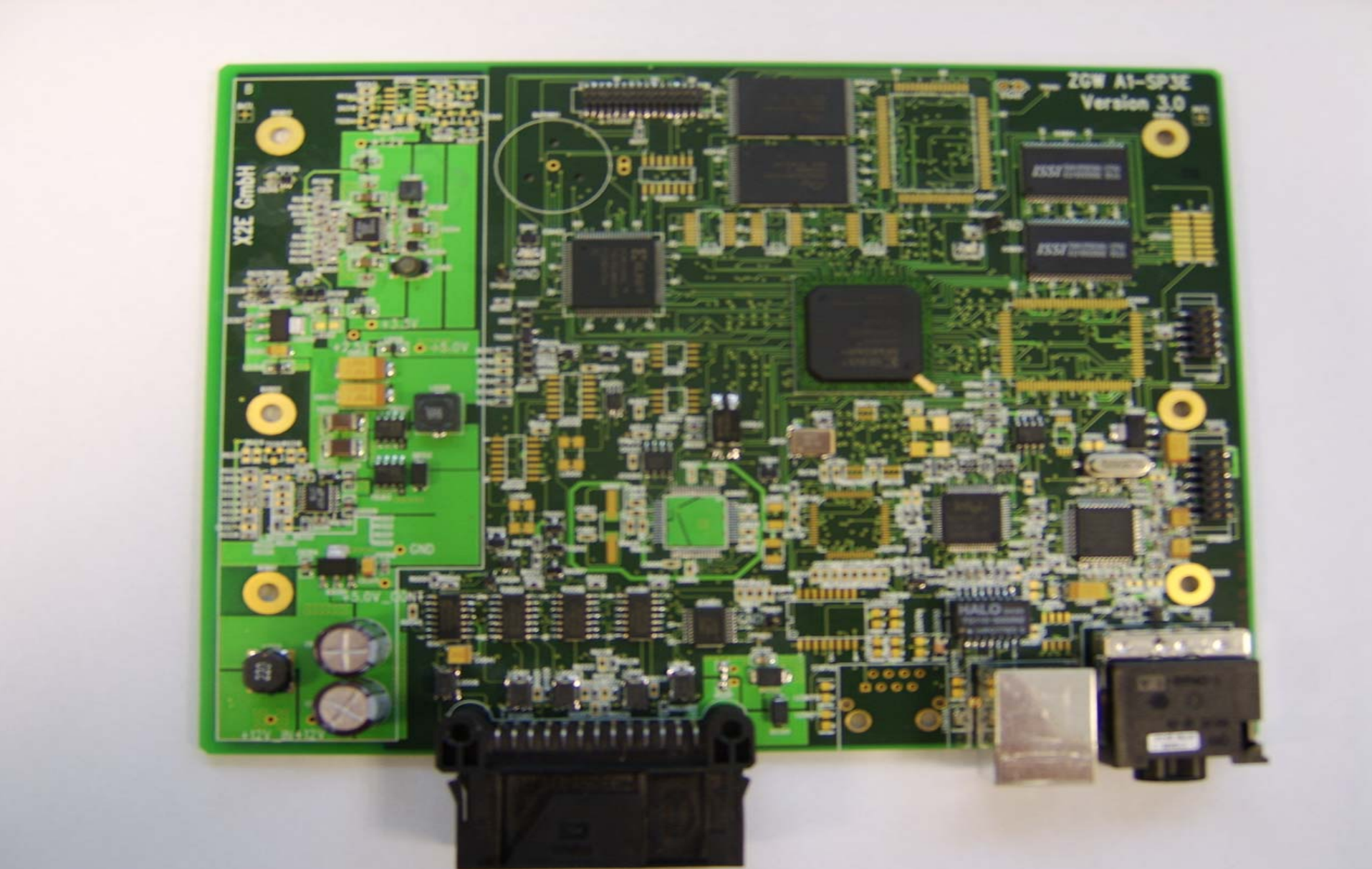
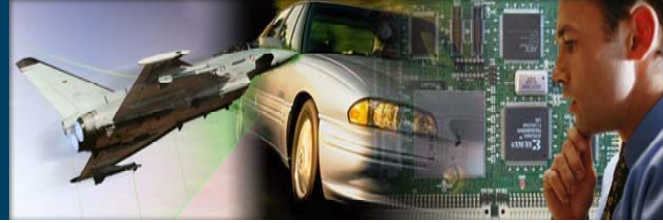
Application Example
Low Cost Gateway



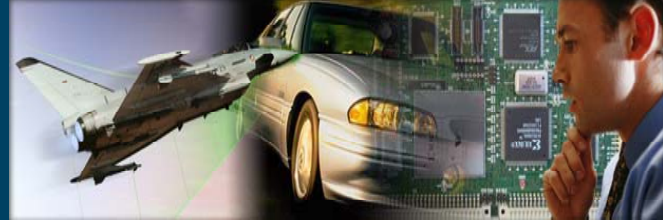


Conclusion



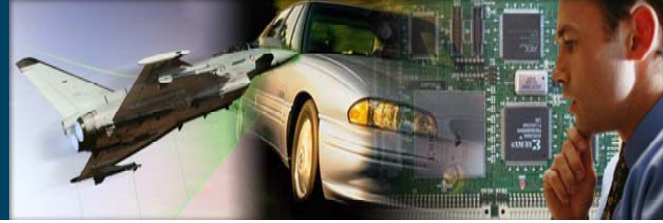
- Most important tasks in the future of embedded system design for automotive:
  - Complex Software Development
  - System Integration
- Necessary: Early target hardware availability
- Solution: FPGA based approaches (SoC FPGA or Low Cost Series) used for mass production:
  - FPGA enables high degree of design re-use and adaption to future products
  - FPGA provides a very good opportunity to solve the device obsolete problem (long term availability, simple re-map to new devices)

Outlook



- Totally programmable hardware based on low cost FGPAs
  - System architectures based on soft processors and IP cores
  - Highly re-useable software stacks
- Entire System composed by hardware and software will become „soft“
- FPGA technology: Cost competitive to traditional ASIC solutions
- OEMs and suppliers become more independence from silicon providers

Dr. Karlheinz E. Weiss
CEO X2E GmbH



Dr. rer.nat. Karlheinz E. Weiss, Dipl. Ing.
age: 40 Years

Curriculum Vitae

10/1986 – 09/1992	Technische Hochschule (TH) Karlsruhe, Germany: major: EE, concentration in integrated circuits and embedded systems, degree: Diplom-Ingenieur (approx. equivalent to an MSEE)
10/1192 – 07/1995	Development engineer at hyperstone electronics, Konstanz, Germany, microprocessor chip design and embedded systems
07/1995 – 02/2001	Scientist at the Wilhelm-Schickard-Institute for Informatics at the University of Tübingen and at the FZI (Computer Research Center) at the University of Karlsruhe, Germany
1997 – 2001	Development of the first generation of car infotainment platform together with Harman/Becker at the FZI, founding of the X2E core design team consisting of five engineers and a couple of electronic students, design of the first generation of the SPYDER-System
12/1999	Received a Doctor (Dr.rer.nat) in technical computer science from the University of Tübingen, subject: *„Architecture design and emulation of embedded systems “*
02/2001 – 03/2005	Elektroniksystem und Logistik-GmbH (ESG) in Munich, Head electronic system design, system architect for the car infotainment platform altern.IS, responsible for the business and development model as well as marketing and technical sales
Since 04/2005	Founder, CEO and Embedded System Architect, X2E GmbH, Kandel/Rheinland-Pfalz