
Analysis of the XC6000 Architecture for Embedded System Design

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Outline

m **Introduction**

- **Explanation of the term “Embedded System”**
- **ASICs and the rule of FPGAs**

m **FZI internal rapid prototyping environment**

- **Microcontroller Board**
- **Add-on Boards**

m **ATM Monitor Application**

m **Two step evaluation process**

- **CTR method on two different architectures (XC4000 and XC6000)**
- **XC6000 architecture, two different methods (CTR and Local RTR)**

m **Results**

m **Summary**

m **Future Work**



Introduction

m **Embedded System**

- **Different application areas demand their own system architecture**
- **Communication technology and industrial automation**
- **Application specific software running on a microcontroller**
- **Application specific hardware (ASICs and FPGAs), communicates with microcontroller and environment via complex interfaces**

m **ASIC**

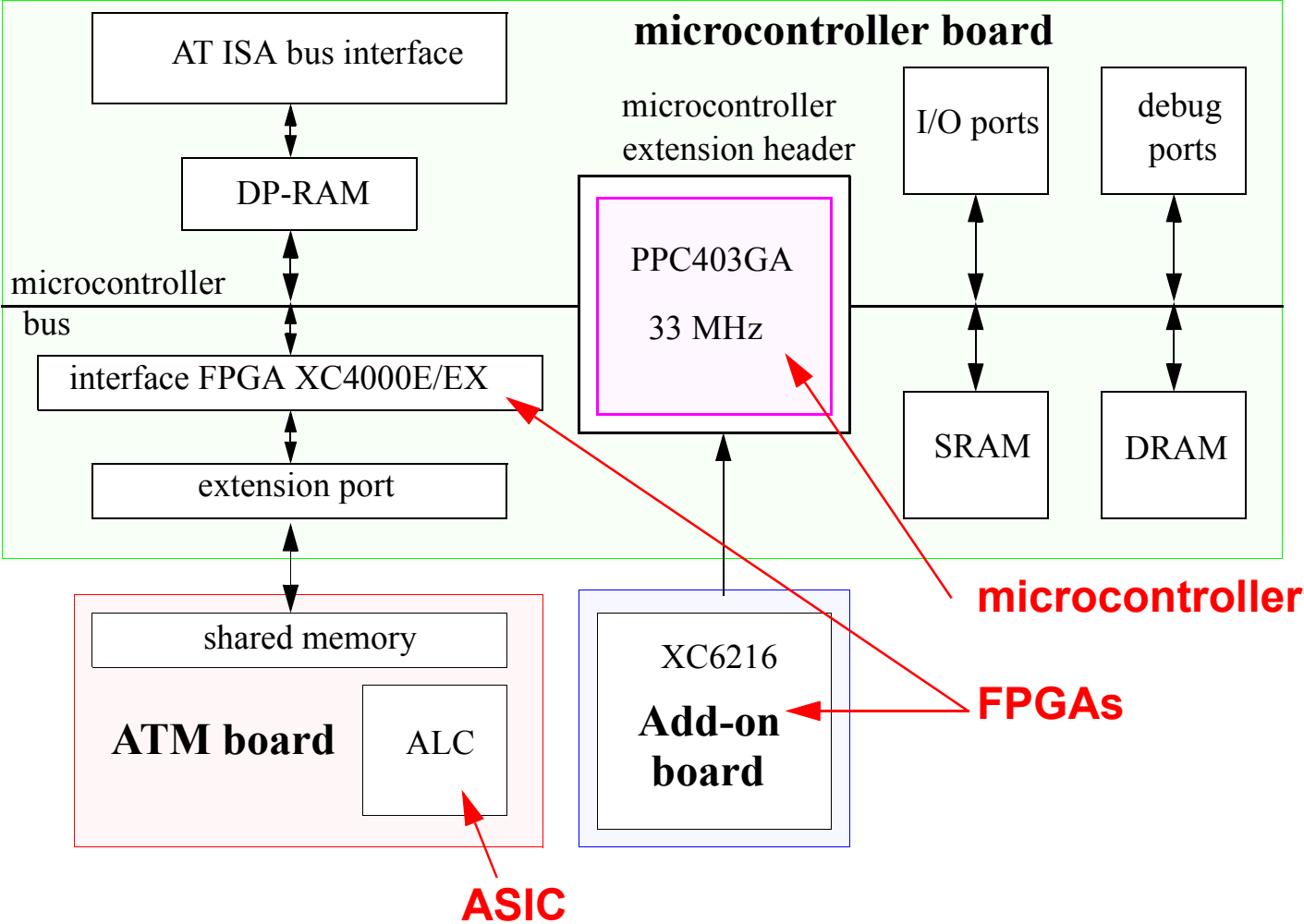
- **Free available VLSI-Chip, that executes an application specific task in hardware (like ATM-ALC)**

m **The rule of FPGAs**

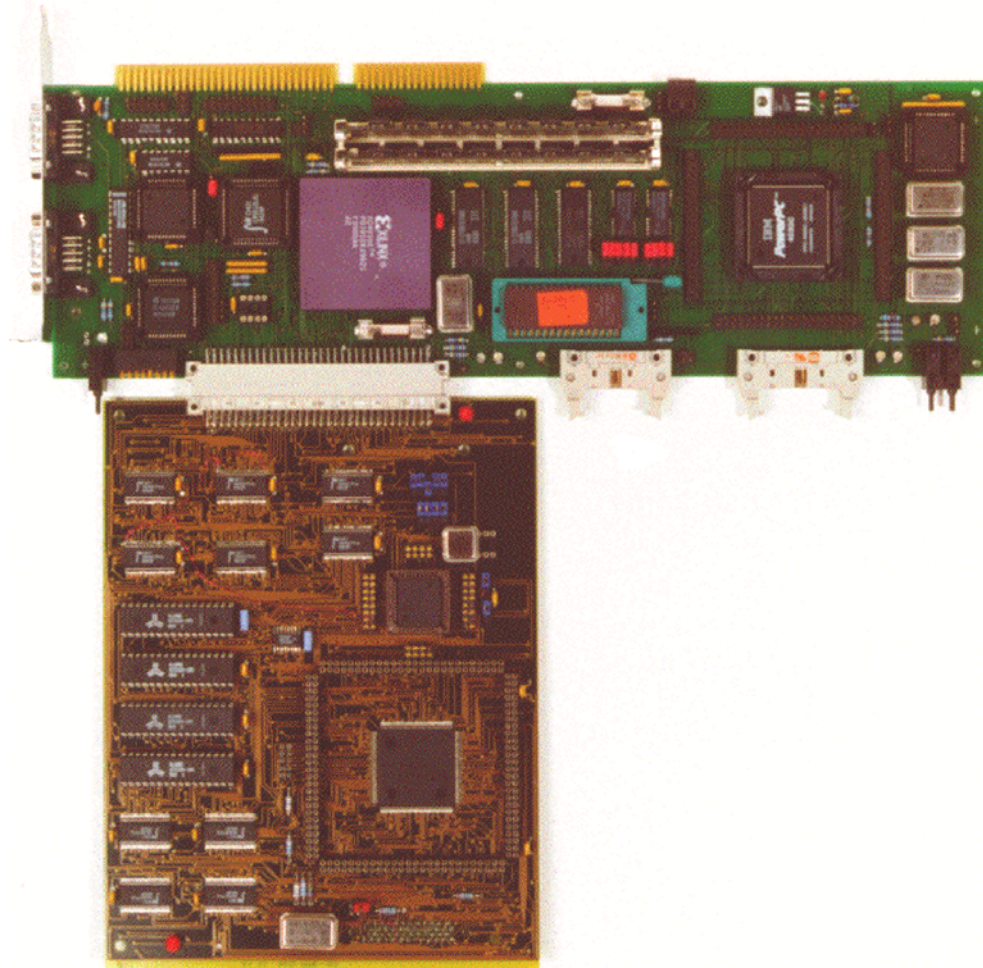
- **Bridging the gap between microcontroller and ASIC (glue logic)**
- **Dedicated hardware, unavailable as an ASIC (“doing the rest”)**



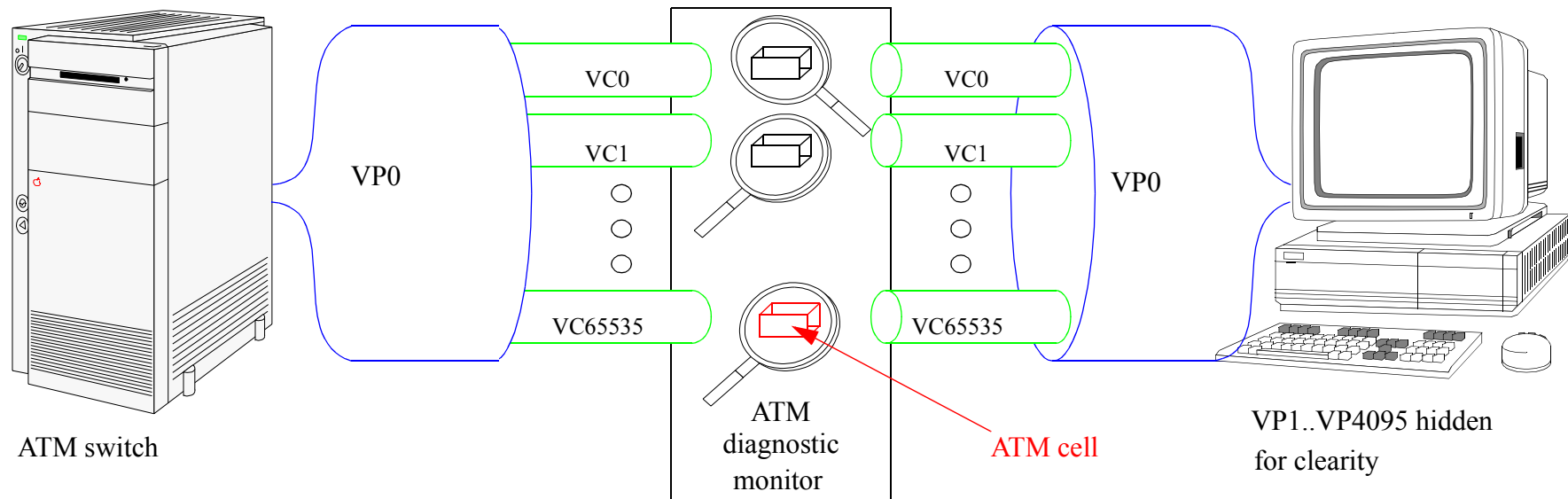
FZI Internal Rapid Prototyping Environment



FZI Internal Rapid Prototyping Environment



ATM Monitor Application: General



- m **4096 Virtual Paths (VP0..VP4095)**
 - each VP subdivided into 65536 Virtual Channels (VC0..VC65535)
- m **coded with 28 bit in the ATM cell header**
- m **serial bandwidth 155Mbit/sec**

ATM Monitor Application: Main Feature

- m **Faulty ATM cells can occur on every Virtual Channel**
 - **Must be detected and counted in dependence of their Virtual Path and Virtual Channel number (28 Bit)**
 - **Worst case every 2.73 μ s (about 90 PPC403 clock cycles)**

- m **Hard real time conditions**
 - **Software solution too slow**

- m **Hardware support through dedicated Error Counter**
 - **Each Error Counter will be initialized to count on a dedicated Virtual Channel**
 - **The monitor should be able to observe “as many Virtual Channels as possible”**
 - **The number of simultaneously running Error Counters is the “hardware functionality”**



ATM Monitor Application: Basic Components

- m **Microcontroller (Embedded PowerPC 403GA)**
 - Initialization process for FPGA and ASIC
 - Set up common data structures in shared memory during booting
 - Updating and controlling of the data structures during run time

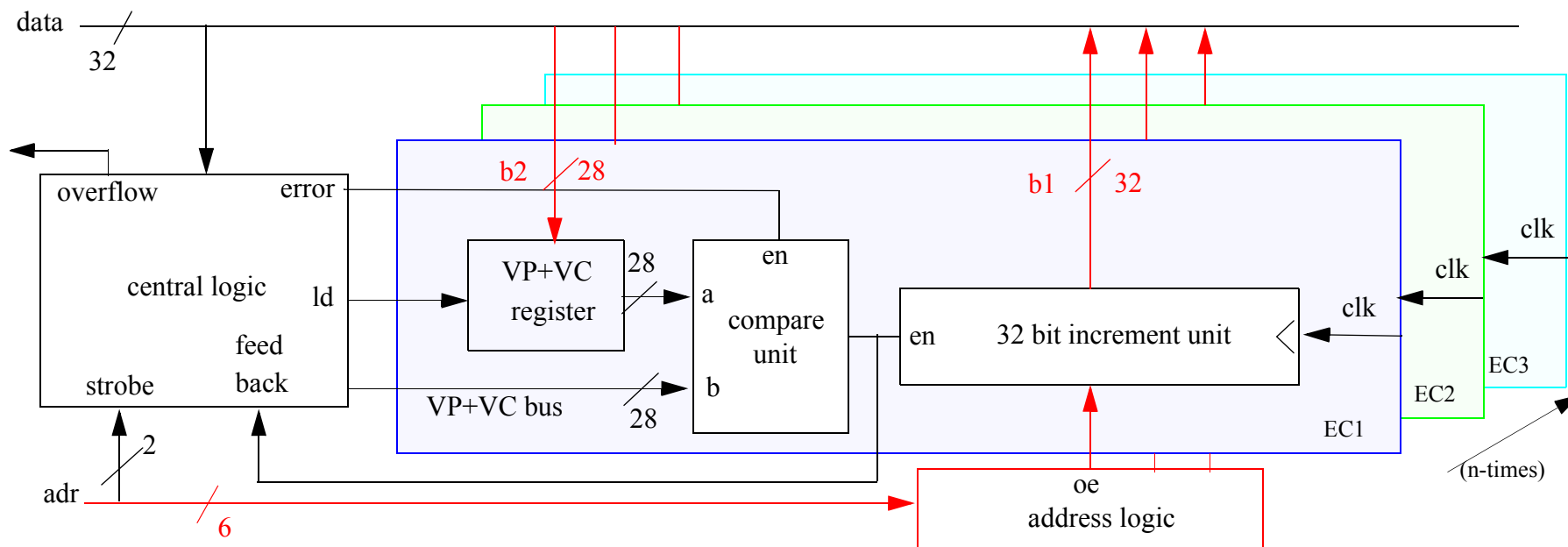
- m **ASIC (Adaption Layer Controller ALC)**
 - Segmentation and reassembly
 - Dedicated error checking in real time

- m **FPGAs (XC4000 or XC6000)**
 - Complex interface between microcontroller and ALC-ASIC (glue logic)
 - Error Counters (“doing the rest”)

-> Which FPGA architecture and implementation method?



Two Step Evaluation Process

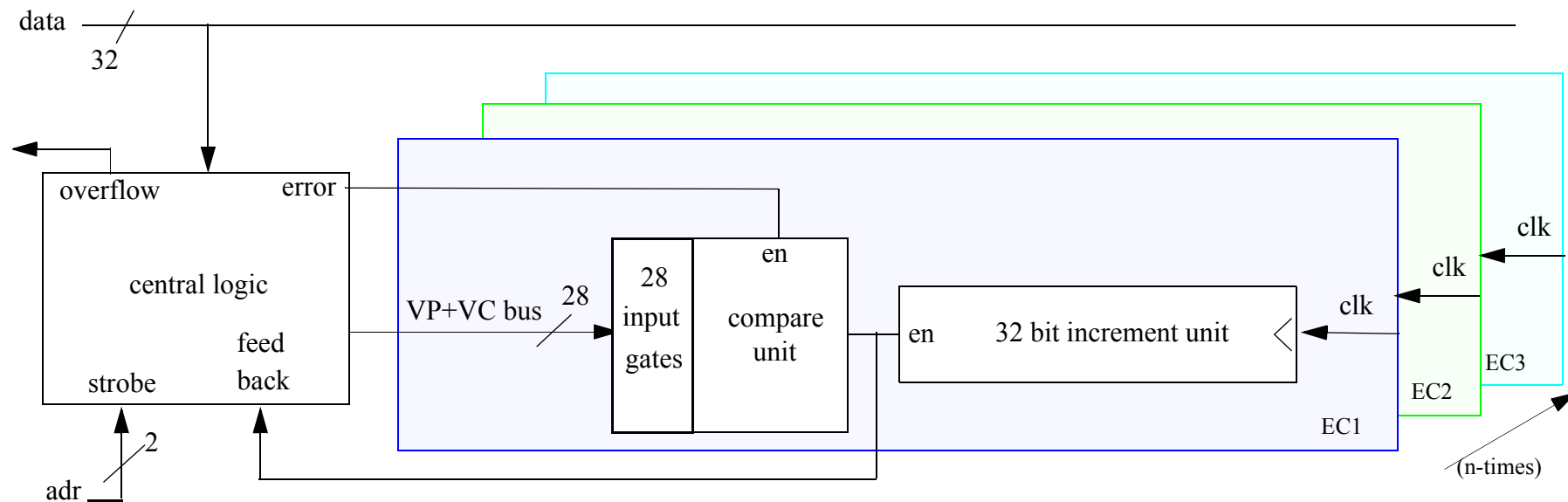


m **First step: Using the CTR method and changing the architecture from XC4000 to XC6000**

-> Advantage: All flip flops can be accessed without any routing resources



Top Step Evaluation Process



m **Second step: Using the same XC6000 architecture and changing the method from CTR to Local RTR**

-> Advantage: Logic gate reduction through constant propagation

Results: CTR Implementation

#EC	10	12	14	16	18	20	24
CLBs	505	611	724	817	898	1023	1219
Device	4020E	4025E	4028EX	4028EX	4028EX	4028EX	4036EX
CLB Utilization	64%	59%	70%	79%	87%	99%	94%
FF Utilization	29%	27%	31%	35%	39%	44%	43%

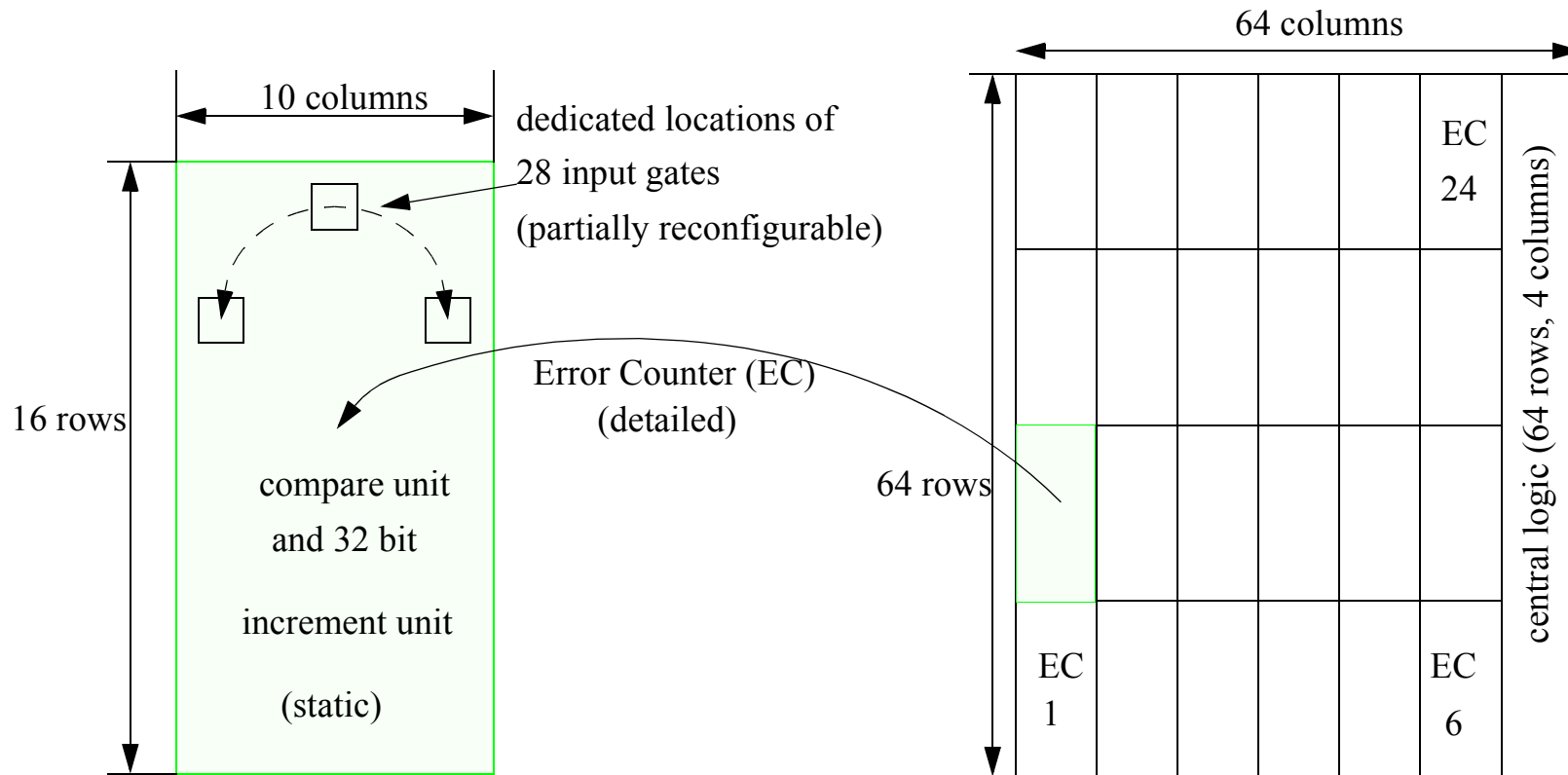
Table 1: Number of Error Counters on different XC4000E/EX devices

- m **CLB Utilization on 4020E and 4025E devices reaches only up to 64%**
 - **CLB Utilization on 4028EX up to 99%, 20 Error Counters implemented**
 - **4028EX provides a typical average gate range of 32.000**

- m **20 Error Counters could be implemented on one XC6216**
 - **XC6216 provides a typical average gate range of 20.000**
 - **XC6216 provides a 60% higher hardware functionality as XC4028EX**

Results: Local RTR Implementation

- m **Up to 24 Error Counters can be implemented on a XC6216 Chip**
- m **Local RTR increases the number of Error Counters by 20% in contrast to CTR on the same XC6216 chip**



Summary

- m **This work evaluates the XC6000 architecture in contrast to the XC4000EX architecture and their related implementation methods**
- m **Our recently completed ATM diagnostic monitor project serves as an industrial benchmark example**
- m **Two step evaluation process:**
 - **Using the same CTR method and changing from XC4000E/EX to the XC6000 architecture will improve the hardware functionality for gates by about 60%**
 - **Using the same XC6000 architecture and changing the implementation method from CTR to RTR will improve the hardware functionality by another 20%**
- m **The evaluation process is based on the FZI internal rapid prototyping environment**



Future Work

- m **Redesign of our microcontroller board**
 - **Implementation of a Real Time Operating System (RTOS-VxWorks)**
 - **Extending interfaces (10Mbit Ethernet, B-ISDN)**
 - **Global RTR support for the XC4000 FPGA**

- m **RTOS support for the XC4000 and XC6000 FPGAs**
 - **Download of FPGA images via RTOS routines during run-time (XC4000)**
 - **Exchange of hardware modules during run-time (XC6000)**

